Speedbridge Megafunction

Solution Brief 13 **January 1997, ver. 1**

Target Application:
Communications

Family:
FLEX 10K and FLEX 8000

Vendor:

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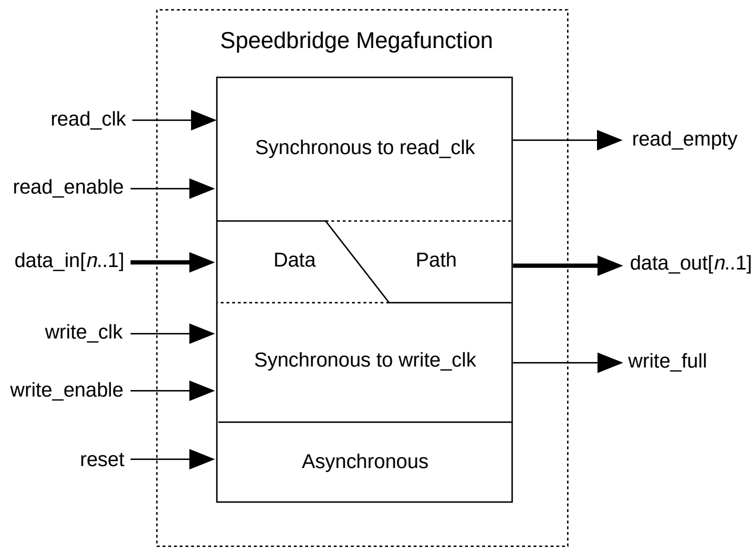
Features

- Optimized for Altera® FLEX® 10K and FLEX 8000 device families
- Eliminates development of an asynchronous first-in first-out (FIFO) buffer
- Independently clocked write and read interfaces
- Configurable widths and depths
- Full and empty status flags

General Description

The SIS Microelectronics Speedbridge megafunction is a speed-matching FIFO buffer that can transfer data across an asynchronous interface. In the megafunction, the read and write ports have independent clocks and synchronous enables for accessing their respective functions. These features allow the clocks to run without triggering read or write operations. The Speedbridge megafunction addresses the need for an asynchronous FIFO, which helps to minimize system development and debugging time and to reduce development cost and design risks. Figure 1 shows a block diagram of the Speedbridge megafunction.

Figure 1. Speedbridge Megafunction Block Diagram



Functional Description

The Speedbridge megafunction receives data synchronous with `write_clk` and ensures that `data_out[n..1]` is synchronous with `read_clk`. At a maximum frequency of one write per clock cycle, the megafunction's specified depth will be fully used. However, if the `write_enable` input is transferring data at a slower rate than one write per clock cycle, and data is being read at a slower rate, the megafunction will become "full" at one data word less than the specified depth.

The megafunction does not contain overflow or underflow flags. However, these flags can be identified outside the megafunction through the `write_full` or `read_empty` outputs. If `write_full` and `write_enable` are high, an overflow error will occur on the next write cycle, and the new data on `data_in[`*n*`..1]` will be lost. If `read_empty` and the `read_enable` are high, an underflow error will occur on the next read cycle, and the data present on `data_in[`*n*`..1]` at the time of the underflow will be undefined.

Ports

Table 1 describes the Speedbridge megafunction's ports.

Table 1. Speedbridge Megafunction Ports

Name	Type	Description
`write_clk`	Input	Clock input. This input can run at any frequency (depending on the range set by the FLEX device architecture), independent from the frequency of the `read_clk` input.
`write_enable`	Input	This input is synchronous with the `write_clk` input. When `write_enable` is high and `write_full` is low, data is written to the megafunction on the rising edge of `write_clk` input.
`reset`	Input	Asynchronous power on reset.
`data_in[`*n*`..1]`	Input	This data input bus is synchronous with the `write_clk` input.
`read_enable`	Input	This input is synchronous with the `read_clk` input. When `read_enable` is high and `read_empty` is low, valid data can be read from the megafunction.
`read_clk`	Input	Clock input. This input can run at any frequency (depending on the range set by the FLEX device architecture), independent from the frequency of the `write_clk` input.
`write_full`	Output	This output is synchronous with the `write_clk` input. When `write_full` is high, `write_enable` is ignored, and no additional data is stored until `write_full` goes low.
`data_out[`*n*`..1]`	Output	This data output bus is synchronous with the `read_clk` input. Data words will be present for a minimum of one `read_clk` cycle, plus a minimum output hold time, and minus a maximum output delay.
`read_empty`	Output	This output is synchronous with the `read_clk` input. When `read_empty` is high, `read_enable` is ignored and data should be considered invalid. Once `read_empty` goes low, data should be considered valid.

Utilization

Table 2 lists the typical device utilization for several Speedbridge megafunction sizes. SIS Microelectronics will customize the megafunction's width and depth according to user specifications.

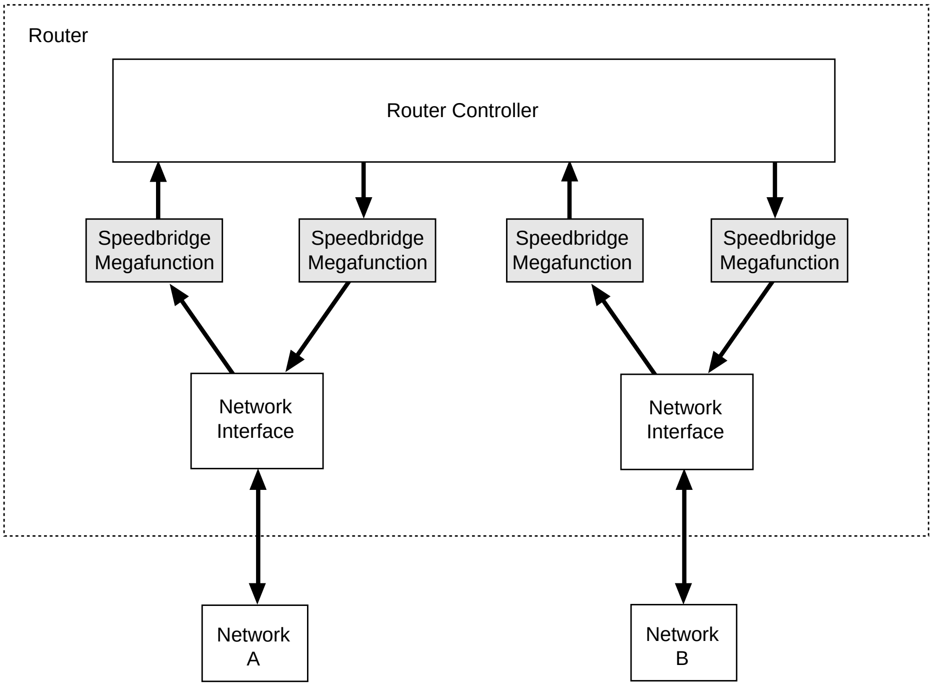
Table 2. Typical Device Utilization for the Speedbridge Megafunction

Depth × Width	Logic Cells Used
4 bits × 8 words	90
8 bits × 8 words	195
16 bits × 8 words	389
32 bits × 9 words	800

Application

Speedbridge megafunctions can be used in a router controller application that provides a network interface between different networks, each running different protocols with different speed and bandwidth characteristics. Inserting a Speedbridge megafunction between the router controller and each network interface eliminates asynchronous timing problems. The router controller and network interface blocks can be designed as independent synchronous blocks, each with its own clock domain. Figure 2 shows several megafunctions used in a network router application.

Figure 2. Speedbridge Megafunctions in a Network Router Application



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